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Performance Analysis of Sincgars Waveform Processing on the Programmable Radio Platform

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The US military is defining new radio requirements that call out military radios implemented digitally in software on commercial technology based platforms. The new radios will be programmable multimode systems capable of hosting any current waveform and future capabilities. Current radios are custom hardware dedicated to one type of waveform and processing capability.

One major risk area is in the area of real-time performance. Commercial hardware and software do not provide the processing power of dedicated hardware designs. Processor utilization and data latency are the two largest risk areas.

A simple architecture utilizing one digital signal processor for MODEM functions, a general purpose processor for data processing and a compact PCI bus for communication was defined. The architecture was taken from material created for a government forum on Programmable Modular Communication Systems.

A discrete event simulation using the Arena simulation tool was created of the US Army’s SINCGARS waveform implemented on the simple model of the processor architecture. Processing times were estimated from processor instruction times, along with estimates of instruction counts for the operations. Input data was derived from data collected during the Army’s Task Force XXI digital battlefield exercises held in 1997. Voice and digital data message traffic logged during the exercise was analyzed to determine arrival rate and message length statistics for the simulation’s traffic generators.

The use of the simulation showed that the SINCGARS waveforms can be easily hosted on COTS processors and up to 3 channels can be configured at a time. The major limitation was CPU utilization of the MODEM digital signal processors during data or voice receptions. All latency requirements can be easily met.